What is claimed is:

1. A semiconductor integrated circuit device comprising:

a hard macro containing a first memory controller that controls the input/output from and to an external memory;

a second memory controller that is provided outside the hard macro and controls the input/output from and to the external memory;

an IO pad unit provided outside the hard macro as an electrical interface to the outside;

a first wiring that connects the first memory controller and the IO pad unit; and

a second wiring that connects the second memory controller and the IO pad unit and has a length shorter than the length of the first wiring.

2. A semiconductor integrated circuit device according to claim 1, wherein the hard macro further includes a CPU.

3. A semiconductor integrated circuit device according to claim 1, further comprising a third wiring that transmits to the first memory controller and the second memory controller, an externally-inputted signal for exclusively switching the states of the first memory

controller and the second memory controller to either one of valid and invalid states.

4. A semiconductor integrated circuit device according to claim 1, further comprising:

a register that is provided inside the hard macro and stores a code for exclusively switching the states of the first memory controller and the second memory controller to either one of valid and invalid states; and

a third wiring that transmits the code stored in the register to the first memory controller and the second memory controller.

5. A semiconductor integrated circuit device according to claim 1, further comprising at least a pair of third wirings that transmits signals for switching the settings of the first memory controller and the second memory controller to the first memory controller and the second memory controller.

6. A semiconductor integrated circuit device according to claim 1, further comprising:

registers that are provided inside the hard macro and store codes for respectively switching the settings of the first memory controller and the second memory controller, and

at least a pair of third wirings for transmitting

the codes stored in the registers to the first memory controller and the second memory controller.

7. A semiconductor integrated circuit device according to claim 5, wherein the external memory exists in plural form and the settings are settings for determining an external memory to be controlled, of the plurality of external memories.

8. A semiconductor integrated circuit device according to claim 7, wherein the settings further include settings related to an address space of the external memory determined as an object to be controlled.